Amendments to the Claims:

The following listing of claims will replace any/all prior versions, and listings, of claims in the application, wherein additions are shown in underlined text:

- 1. (Currently amended) A method for forming a bit line of a flash device, the method comprising the steps of:
 - (a) forming a barrier film, an interlayer insulation film, and a metal hard-mask film sequentially on a semiconductor substrate, on which a bit line contact plug is formed;
 - (b) forming a metal hard-mask film pattern for opening a bit line area corresponding to the bit line contact plug;
 - (c) forming a bit line trench;
 - (d) forming a bit line metal film to bury the bit line trench; and,
 - (e) removing the bit line metal film and the metal hard mask film on the interlayer insulation film with a metal material.

wherein the metal hard-mask film and the bit line metal film are formed using the same metal material used in step (e).

- (Original) The method of claim 1, further comprising between steps(c) and (d), a step of cleaning the bit line trench.
- 3. (Original) The method of claim 2, wherein the cleaning step comprises a dry cleaning process using plasma or a cleaning process by high-frequency sputtering.
- 4. (Original) The method of claim 3, wherein the dry cleaning process is performed using a mixed gas of CF₄ and O₂ and NF₃ gas, and the cleaning process by high-frequency sputtering is performed using Ar gas.
 - 5. (Canceled).

- 6. (Original) The method of claim 1, the metal hard-mask film is formed using tungsten (W) with a thickness in the range of 500 Å to 1000 Å to endure significantly as an etching barrier in the subsequent process of etching the interlayer insulation film.
- 7. (Original) The method of claim 1, wherein step (b) comprises patterning the metal hard-mask film.
- 8. (Original) The method of claim 1, wherein step (c) comprises etching the interlayer insulation film and the barrier film using the metal hard-mask film pattern as an etching mask.
- 9. (Currently amended) The method of claim 1, wherein step (e) comprises a planarization process.